Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claim 1 (currently amended). A method for fabricating a buried bit line for a semiconductor memory, which comprises:

~~producing strip-like doped regions parallel to and at distances from one another in a semiconductor body, the regions being adapted to act as bit lines and as source/drain regions of a respective memory transistor;~~

~~applying laterally with respect to the doped regions, in each case, one layer sequence adapted to act as a gate dielectric and including a lower boundary layer, a storage layer, and an upper boundary layer;~~

~~forming an oxide region in each case on a side of the doped regions remote from the semiconductor body, the oxide region being thicker than the lower boundary layer;~~

~~before the upper boundary layer is applied and after the application of the storage layer, applying a sacrificial layer made from a material selectively etchable with respect to a~~

~~material of the storage layer and to polysilicon onto the storage layer;~~

~~producing openings in the sacrificial layer, the storage layer, and the lower boundary layer, extending to the semiconductor body, by using a mask;~~

~~introducing doped polysilicon into the openings;~~

~~removing the sacrificial layer; and~~

~~producing the upper boundary layer on the storage layer and oxidizing at least a proportion of the polysilicon to form the oxide region~~

providing a semiconductor body;

applying a lower boundary layer and a storage layer to the semiconductor body;

applying a sacrificial layer made from a material selectively etchable with respect to the storage layer and to polysilicon onto the storage layer;

producing openings in the sacrificial layer, the storage layer, and the lower boundary layer, extending to the semiconductor body, the openings being produced above regions where buried bit lines are to be produced;

introducing doped polysilicon into the openings;

etching back the polysilicon to a residual portion;

removing the sacrificial layer;

applying an upper boundary layer on a surface of the storage layer and the residual portion of the polysilicon and oxidizing the residual portion of the polysilicon to form an oxide region, the oxide region being thicker than the lower boundary layer, the lower boundary layer, the storage layer and the upper boundary layer acting as a gate dielectric;

forming a diffusion region in the semiconductor body below the oxide region during the oxidation of the residual portion of the polysilicon, the diffusion region forming the buried bit line.

Claim 2 (original). The method according to claim 1, wherein the sacrificial layer is produced as a deposited oxide.

Claim 3 (previously presented). The method according to claim 1, which further comprises selecting the storage layer from a group of materials consisting of silicon nitride, tantalum oxide, hafnium oxide, hafnium silicate, titanium oxide, zirconium oxide, aluminum oxide, and intrinsically conductive silicon.

Claim 4 (previously presented). A method for fabricating a buried bit line for a semiconductor memory, which comprises:

producing strip-like doped regions parallel to and at distances from one another in a semiconductor body, the strip-like doped regions being adapted to act as bit lines and as source/drain regions of a respective memory transistor;

applying laterally with respect to the doped regions, in each case, one layer sequence adapted to act as a gate dielectric and including a lower boundary layer, a storage layer, and an upper boundary layer; and

forming an oxide region thicker than the lower boundary layer, in each case, on a side of the doped region remote from the semiconductor body;

before producing the upper boundary layer and after the application of the storage layer, applying a sacrificial layer with a topside to the storage layer;

producing openings with lateral walls in the sacrificial layer, the storage layer, and the lower boundary layer, by using a mask;

introducing dopant into implantation regions of the semiconductor body through the openings;

etching back the lateral walls of the openings and a topside of the sacrificial layer at an etching rate sufficient to form smooth sides on the sacrificial layer, the storage layer, and the lower boundary layer;

removing residues of the sacrificial layer selectively with respect to the storage layer; and

producing the upper boundary layer on the storage layer and forming an oxide region on a free surface of the semiconductor body, in each case between the sides.

Claim 5 (original). The method according to claim 4, which further comprises heating until the dopant introduced into the

implantation regions has diffused to a portion of the semiconductor body covered by the storage layer.

Claim 6 (previously presented). The method according to claim 4, wherein the sacrificial layer is produced as a deposited oxide.

Claim 7 (previously presented). The method according to claim 4, which further comprises selecting the storage layer from a group of materials consisting of silicon nitride, tantalum oxide, hafnium oxide, hafnium silicate, titanium oxide, zirconium oxide, aluminum oxide, and intrinsically conductive silicon.

Claim 8 (new). The method according to claim 1, which further comprises producing spacers at walls of the openings before introducing the polysilicon into the openings.